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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/661,498	09/14/2000	Alnoor M. Shivji	005100.P004	8758
47372	7590	07/08/2005	EXAMINER	
BIRCH, STEWART, KOLASCH & BIRCH, LLP 8110 GATEHOUSE ROAD SUITE 100 EAST FALLS CHURCH, VA 22042-1248			NGUYEN, STEVEN H D	
			ART UNIT	PAPER NUMBER
			2665	

DATE MAILED: 07/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No. .

09/661,498

Applicant(s)

SHIVJI ET AL.

Examiner

Steven HD Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 April 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4/26/05 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 11-12, 14 and 18-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Garg (US 2002/0131442).

Regarding claims 11 and 20, Garg discloses a method in cell which is implemented in array of cells operably connected according to a sequence (Fig 3, Ref 302 is a cell which is coupled to another cell 304 in a sequence of column, See switch module is a cell, Page 7, Sec 67), receiving a bit stream of multiple bits streams at a multiplexer in the implement cell (Fig 7, Ref 702 is multiplexer for receiving a multiple bits stream into an input of multiplexer which contains 32 channels "rails" wherein the signal have a format of STS-1 of Ref 302 of Fig 3) and

selecting at least one bits from a stream of bits to be latched within the implement cell based, at least in part, on a space control register value and time control register value; receiving at the implemented cell (Fig 3, Ref 302) one or more bits output by previous cell in the sequence (Fig 3, Ref 314 receives the output of one or more bit stream from the cell 304) and output an output bits stream includes the selected one or more bits and the one or more bits received from the previous cell (Fig 3, Ref 304) according to the format of output bit map (Fig 7, Ref 702 and 710 used to select at least one bit from the bit stream based one 5 bit rail selection value “space control register value” and 5 bit slot selection value “time control register value” to output an output bit stream having a second format according the output bit map of storage 706 which is different from the input bit stream of first format STS-1; Fig 7, Ref 706, the bit map of 706 implicitly has a different format than the input format of the input stream).

Regarding claim 12, Garg discloses the space control register value indicating a selected stream of data from a plurality of streams of data (Fig 7, Ref 702 uses the input value of 5 bit rail selection for selecting the bits from the multiple bits stream for output to the latch 710).

Regarding claim 14, Garg discloses the time control register value indicating at least one bits from a selected stream of data (Fig 7, Ref 708 uses the input value of 5 bit slot selection for selecting the bits from selected stream for inputting into the latch 710).

Regarding claims 18 and 19, Garg discloses the outputting the second stream of bits includes outputting the one or more bits received from the previous cell during an interval in which no bits are latched by the implemented cell and outputting the one or more selected bits during an interval in which the implemented cell latches the one or more selected bits (Fig 3, ref 314 is used to output bit streams of the implement cell 302 and previous cell 304).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1-7, 10, 13 and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Garg (US 20020131442).

Regarding claims 1 and 17, Garg discloses a circuit comprising an array of cells operably connected according to a sequence (Fig 3, ref 302 and 304, switch module is a cell, Page 7, Sec 67), each cell includes a multiplexer (Fig 7, Ref 702) which has an input for receiving space control register value to control the multiplexer (Fig 7, 5 bit rail selection) and receiving a bit stream having a first format from a plurality of multiple bit streams and a latch (Fig 7, Ref 710) coupled to receive a signal from the multiplexer and a control circuit coupled to control the latch, the control circuit to select at least one bits from stream of bits output by the multiplexer of each of the cells (Fig 7, Ref 708) for generating a second output stream having a second format

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according to the output bit map storage (Fig 7, Ref 706, the bit map of 706 implicitly has a different format than the input format of the input stream) wherein at least one cell in the sequence is coupled to previous cell in the sequence in order to receive one or more bits output by the previous cell (Fig 3, Ref 302 and 304 are the cells which each includes an assembler for receiving the output of the previous cell for outputting. Garg does not fully disclose a space control register. However, it would have been obvious to one of ordinary skill in the art to apply a register for storing the value because it is well known and expected in the art to use a register to store a value for controlling a multiplexer.

Regarding claim 2-5, Garg does not disclose the multiplexer comprising a plurality of multiplexers such as a first, second, third, fourth multiplexer are 8:1 and fifth multiplexer is 6:1 wherein the input of fifth multiplexer coupled to the output of first, second, third and fourth multiplexer. However, it would have been obvious to one of ordinary skill in the art to cascade four 8:1 multiplexers to one 6:1 multiplexer to obtain 32:1 multiplexer because it is well known and expected in the art to cascade the multiplexers. The motivation would have been to increase the input stream to the switch core.

Regarding claim 7, Garg discloses the control circuit comprising a time control register value for indicating a selected bit from a sequence of bits (Fig 7, Ref 5 bit slot selection) and a counter to count bits in the sequence of bits from a predetermined bit (Fig 7, Ref counter) and a comparator for comparing the value of the counter and the value of time control register for generating a load signal to enable the latch to store the value output by the multiplexer (Fig 7, Ref 708). However, Garg does not disclose the time control register for storing the value of time control register. Therefore, it would have been obvious to one of ordinary skill in the art to

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apply a register for storing the value because it is well known and expected in the art to use a register to store a value for using to compare with another value to generate an output value.

Regarding claim 10, Garg does not disclose the multiplexer receiving the logical values to generate alarm signal. However, Garg discloses a space and time switch for carrying the SONET signal that is implicitly disclosed the logical values for using to generate alarm signals.

Regarding claims 6, 13 and 15, Garg does not disclose the space/time control register value being programmable. However, it is would have been obvious to one of ordinary skill in the art to implement a value which is stored in the register to be programmable and programmable register is well known and expected in the art. It is a designer choice. The motivation would have been to allow the manufacture to setup the value according to the network.

Regarding claim 16, Garg discloses the at least one of the cells is configured to output the one or more bits from the previous cell during an interval in which no bits are selected by the least one cell's latch, and output the one or more selected bits during an interval in which the at least one cell's latch selects the one or more selected bits (Fig 3, ref 314 is used to output bit streams of the implement cell 302 and previous cell 304).

7. Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Garg in view of Irwin (USP 5841771).

Regarding claims 8-9, Garg discloses a second multiplexer (Fig 3, Ref 314) for receiving a signal output by the latch and the signal output by the previous cell (Fig 3, Ref 304). However, Garg does not disclose a second control circuit to control the second multiplexer and a second latch coupled to receive a signal output by the second multiplexer. In the same field of endeavor,

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Irwin discloses a second multiplexer is controller by a control circuit (Fig 3, ref 651) and a second latch coupled to receive a signal output by the second multiplexer (Fig 13, Ref 706 is a second multiplexer for receiving out signals from 703 and 615 and for coupling to second latch 617).

Since, Garg suggest the output of first latch is coupled to a second multiplexer having an input for receiving an output of another cell. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to apply a control circuit and a second latch coupled to receive a signal output by the second multiplexer as disclosed by Irwin into Garg's system. The motivation would have been to simultaneously read out the data from storage to reduce transmission delay.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven HD Nguyen whose telephone number is (571) 272-3159. The examiner can normally be reached on 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy D. Vu can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Steven HD Nguyen
Primary Examiner
Art Unit 2665
7/5/05